CLAIMS

1. A method of verifying a digital hardware design simulated in a hardware design language (HDL), including the steps of:

defining at least one state to be verified, the state including a signal value for each of a plurality of components within the hardware design;

applying a test to the hardware design;

generating traces of internal signals within the hardware design during the test, each trace including signal data and time data and including at least the internal signals associated with the components;

processing the traces to ascertain whether the plurality of components simultaneously had the signal values associated with the state, thereby to ascertain whether the state was achieved.

2. A method according to claim 1, wherein more than one state is defined, each state having a signal value for each of a plurality components of the hardware design, the traces being processed to ascertain, for each state, whether the corresponding plurality of components simultaneously had the signal values associated with the state, thereby to ascertain whether each of the states was achieved.

3. A method according to claim 2, wherein the processing step includes ascertaining whether a predetermined sequence of states was achieved.

4. A method according to claim 3, wherein the processing step includes ascertaining whether a given state in a sequence was achieved within a predetermined time period after an earlier state in the sequence.

5. A method according to claim 1, wherein the traces are pre-processed prior to the processing step, such that, for at least each of the components defined within each of the states, a value for the respective signals associated with those components exists for each time for which the traces are to be processed.

6. A method according to claim 1, wherein one or more of the signal values are values of a field associated with the corresponding component.